

HW-CLK-104


SUPERCLOCK RF3 MODULE

Disclaimer:

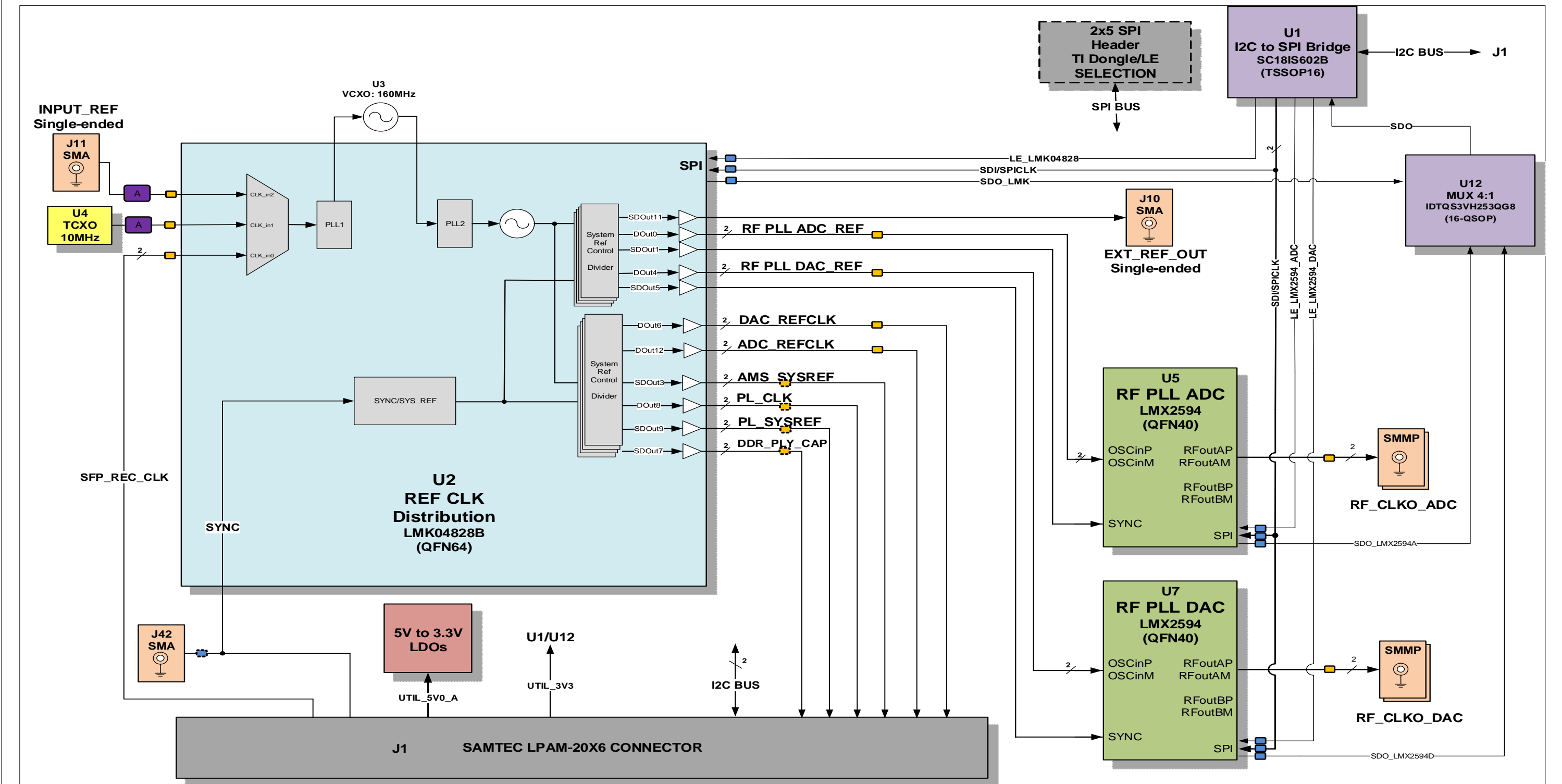
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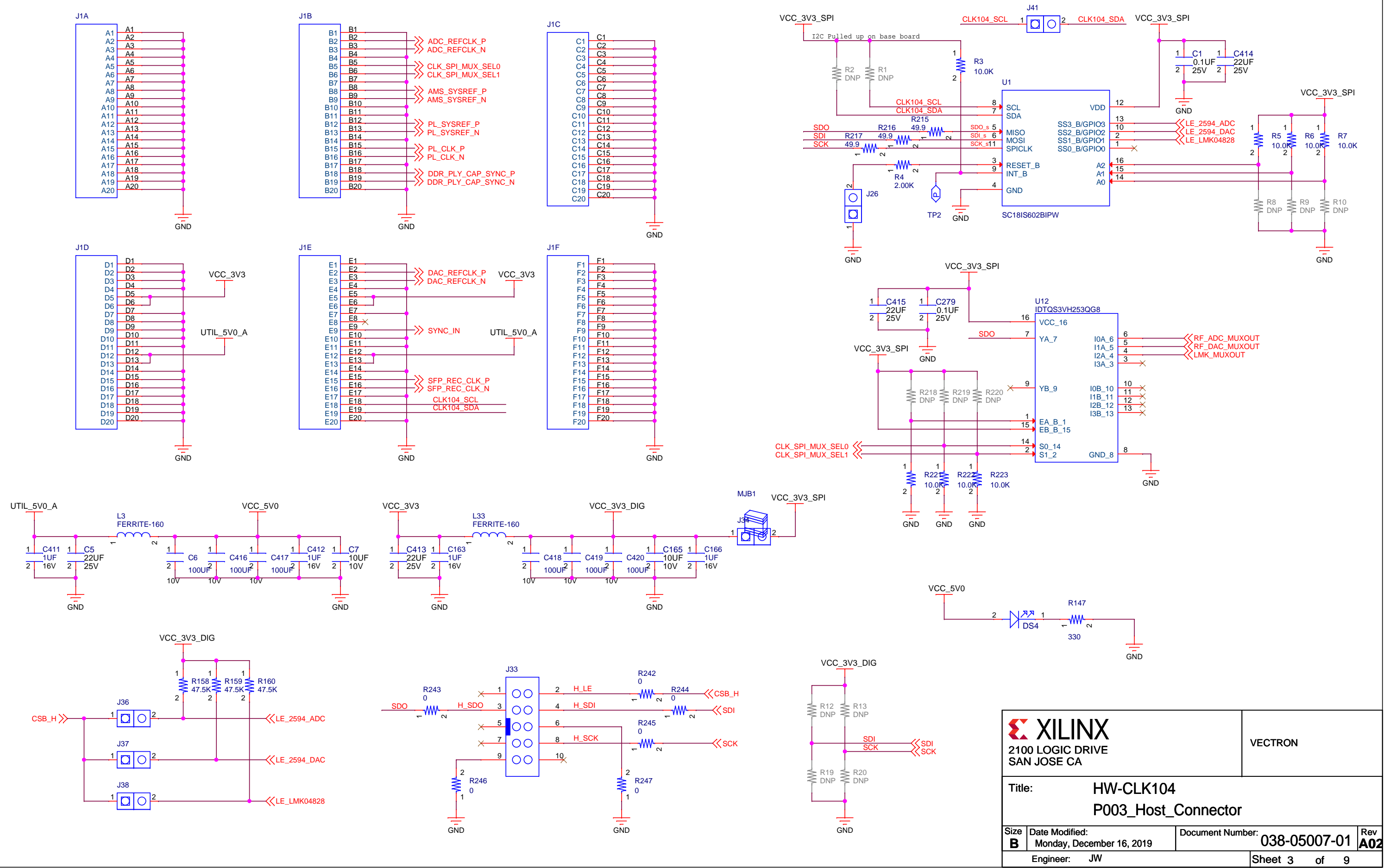
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Block Diagram



HOST CONNECTOR



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The image shows a detailed PCB layout for the LMK04828 evaluation board. The layout is organized into several functional blocks:

- Power Input and Distribution:** The top left shows the VCC_4828_VCO input, which branches into VCC_3V3_DIG and VCC_4828_VCO. These are connected to various decoupling capacitors (C185, C21, C23, C186, C187, C28, C27, C188, C190, C480, C31, C191) and inductors (L5, L6, L8) to provide stable power to the VCO and digital logic.
- OSCILLATOR SECTION:** The VCC_4828_OSC section includes capacitors C40 and C196, connected to the oscillator input.
- REFERENCE AND BUFFER SECTION:** The VCC_4828_BUF1, VCC_4828_BUF2, and VCC_4828_BUF3 sections provide clean reference voltages for the buffers. These are connected to capacitors C398, C399, C400, C401, and C402.
- CP2 and PLL2 SECTION:** The VCC_4828_CP2 and VCC_4828_PLL2 sections include capacitors C48, C200, C56, and C202, connected to the CP2 and PLL2 inputs.
- OUTPUT AND STATUS SECTION:** The bottom right shows the output of the LMK04828, including the SFP_REC_CLK_P and SFP_REC_CLK_N signals, the CLK_IN1_ATT signal, and the CLK_4208_IN1_CMOS signal. It also includes status signals like RESET, CLKN_SEL0, CLKN_SEL1, CS, SCK, SDI, STATUS_LD1, and SYNC.

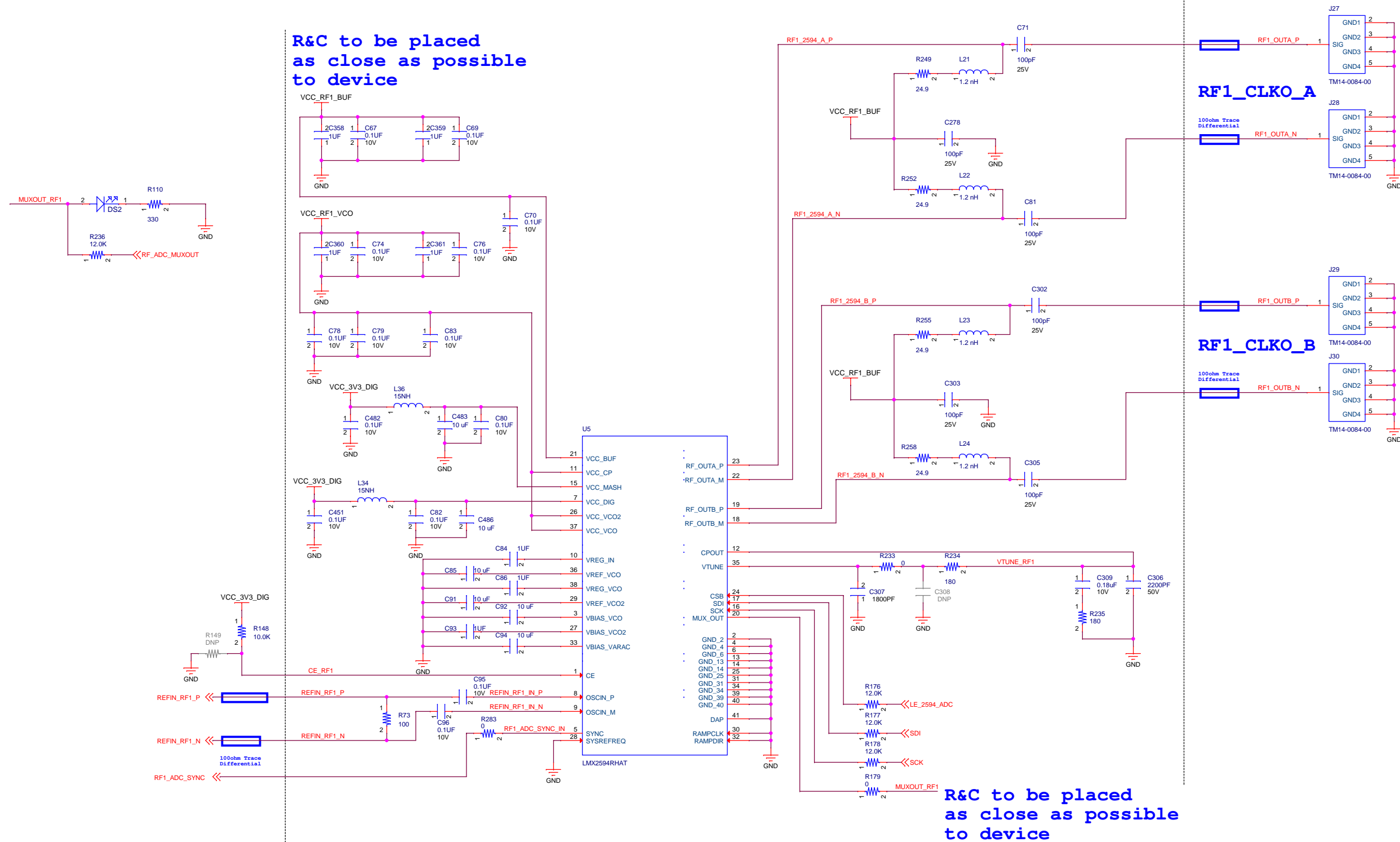
The layout uses a color-coded system to identify different power planes and signal traces. The components are labeled with their respective values and footprints, and the board is populated with various passive components like capacitors, inductors, and resistors.

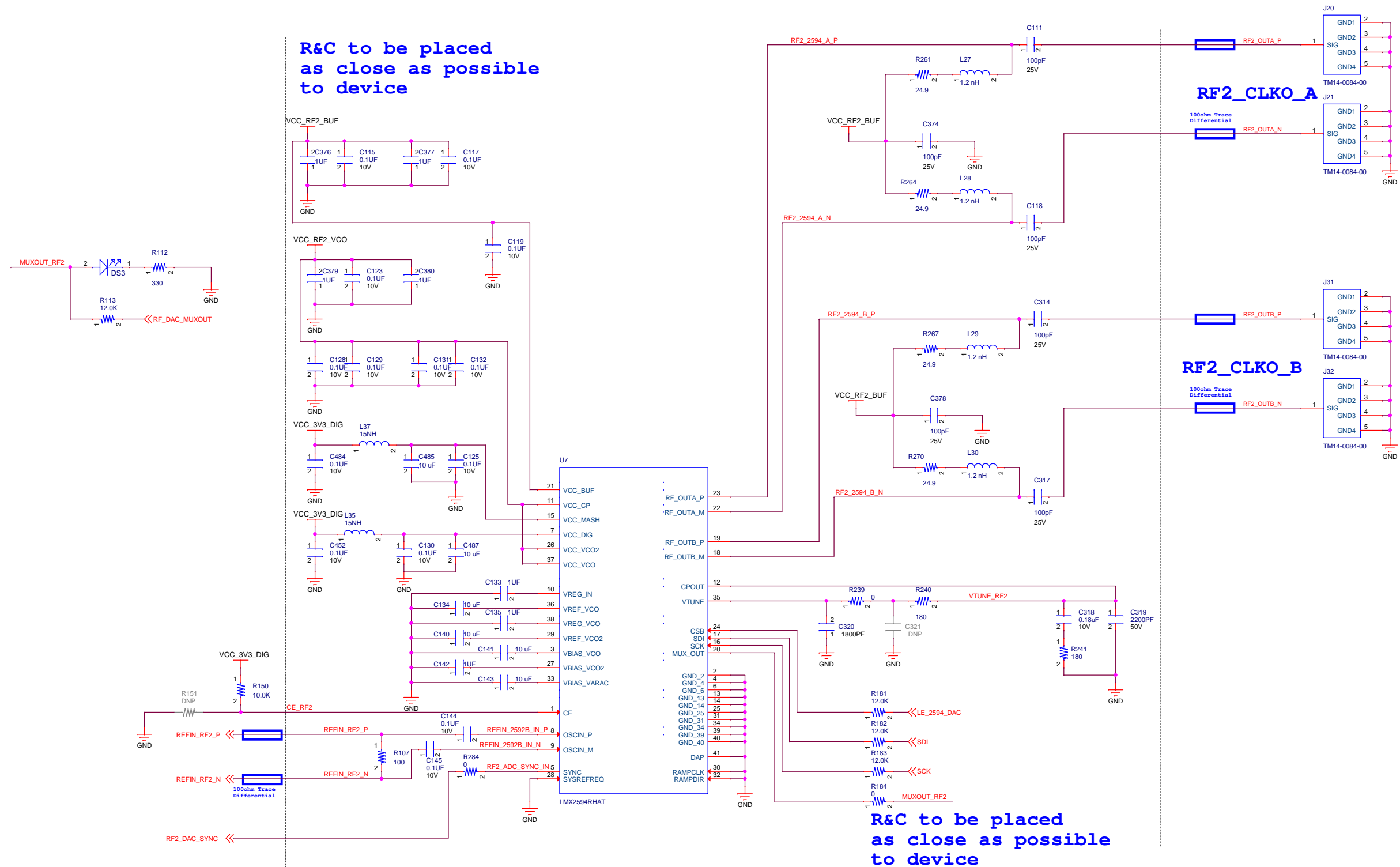
Module	Signal	Direction	Notes
MC_7	SDCLK_OUT0_N		
	SDCLK_OUT5_P		
MC_8	SDCLK_OUT5_N		
	SDCLK_OUT3_P		
MC_9	SDCLK_OUT3_N		
	DCLK_OUT12_P		
REF	DCLK_OUT12_N		
	DCLK_OUT6_P		
MC_10	DCLK_OUT6_N		
	DCLK_OUT9_P		
MC_11	DCLK_OUT9_N		
	DCLK_OUT4_P		
MC_12	DCLK_OUT4_N		
	DCLK_OUT8_P		
MC_13	DCLK_OUT8_N		
	SDCLK_OUT8_P		
MC_14	SDCLK_OUT8_N		
	DCLK_OUT10_P		
MC_15	DCLK_OUT10_N		
	SDCLK_OUT11_P		
MC_16	SDCLK_OUT11_N		
	DCLK_OUT2_P		
MC_17	DCLK_OUT2_N		
	SDCLK_OUT7_P		
MC_18	SDCLK_OUT7_N		
	SDCLK_OUT13_P		
MC_19	SDCLK_OUT13_N		
	STATUS_LD2		

R&C to be placed as close as possible to device

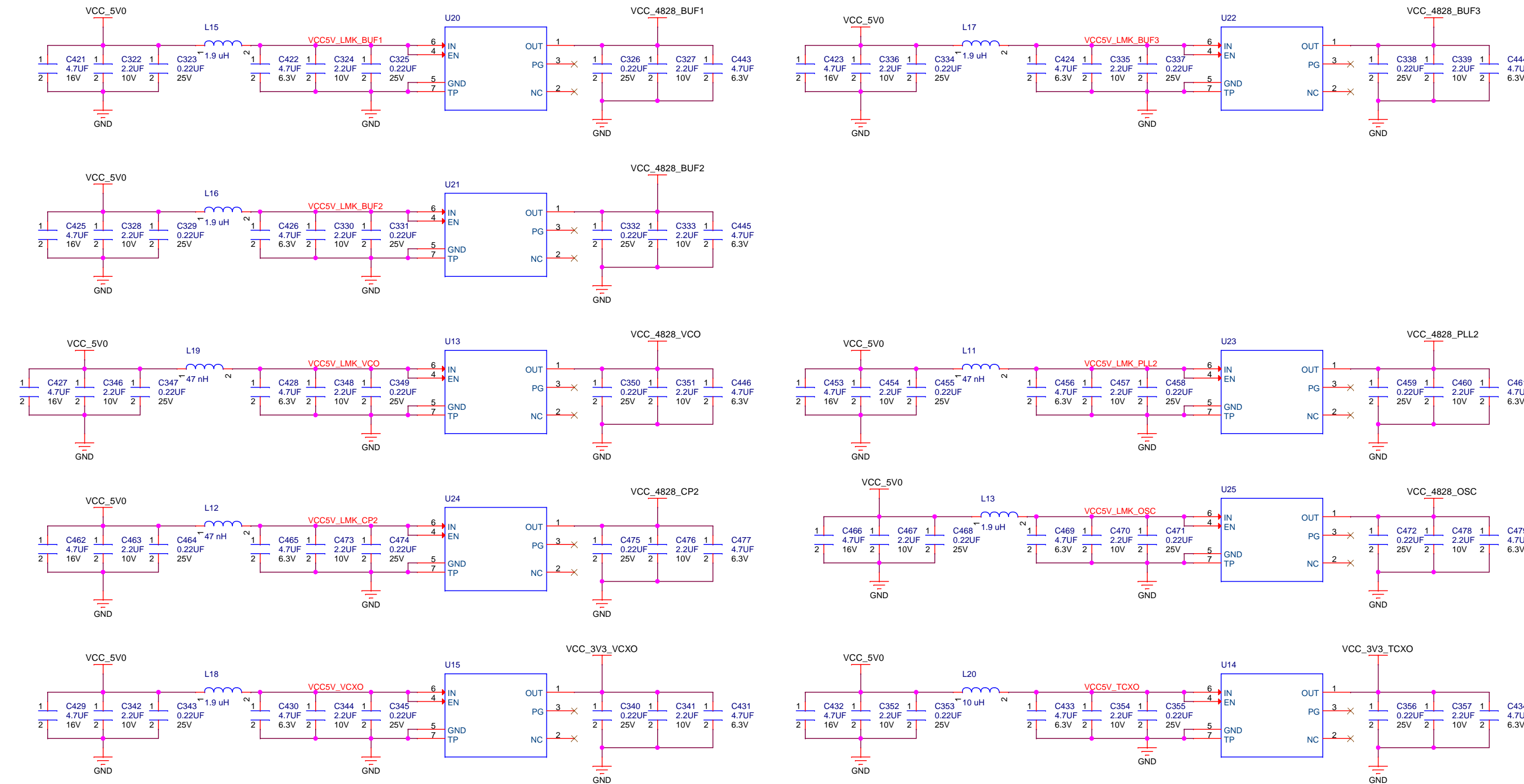
EXTERNAL INPUT

10~20MHz
Single-ended

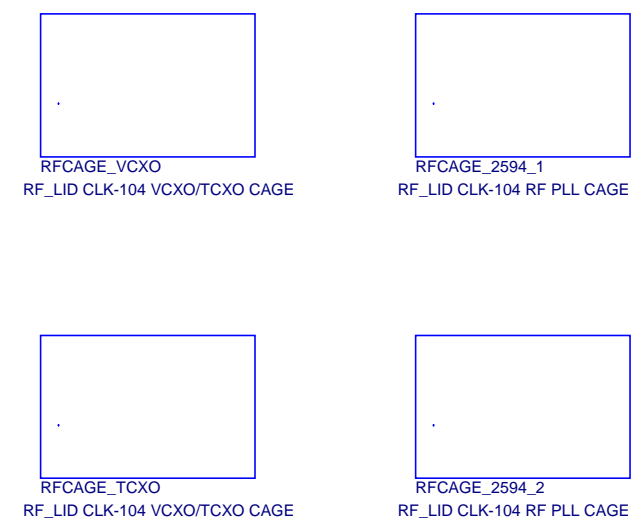
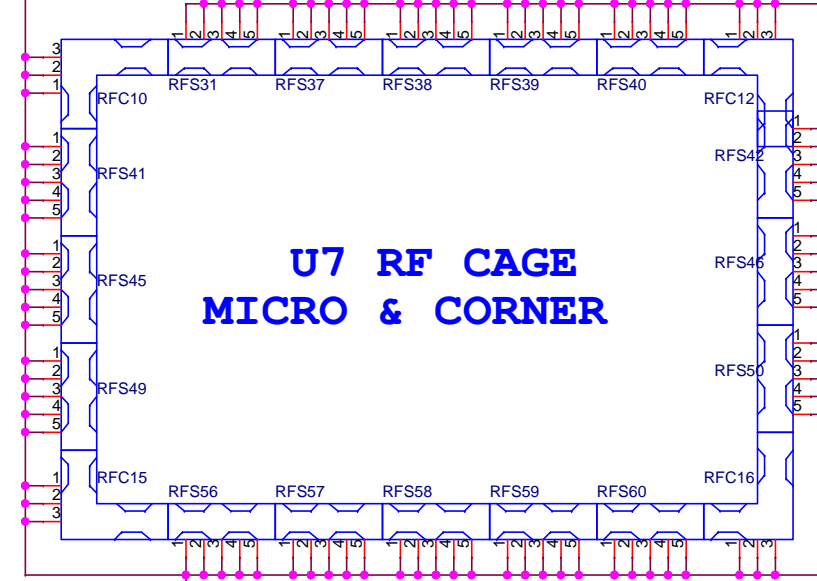
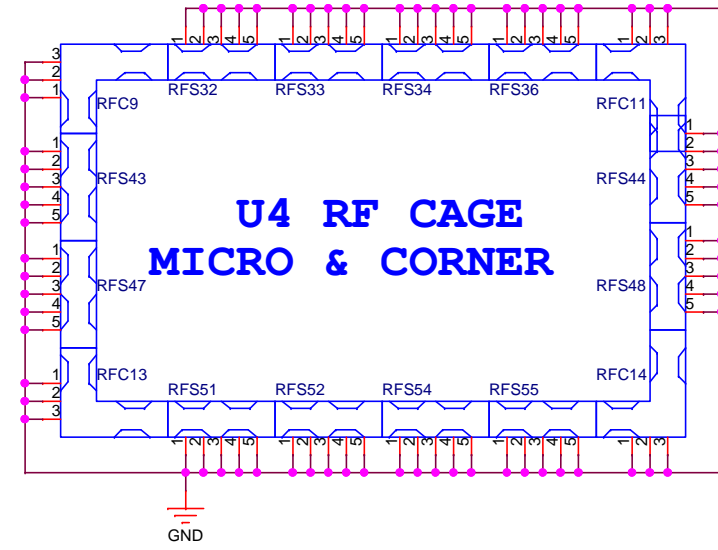
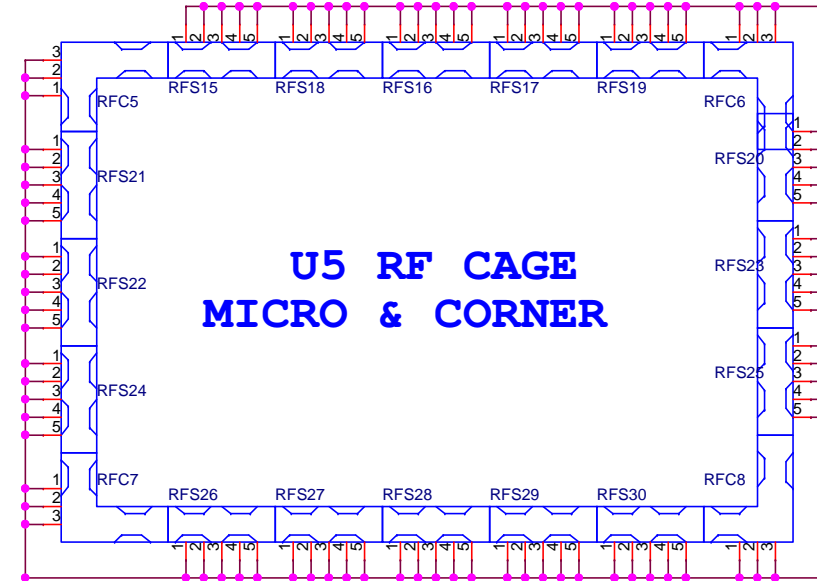
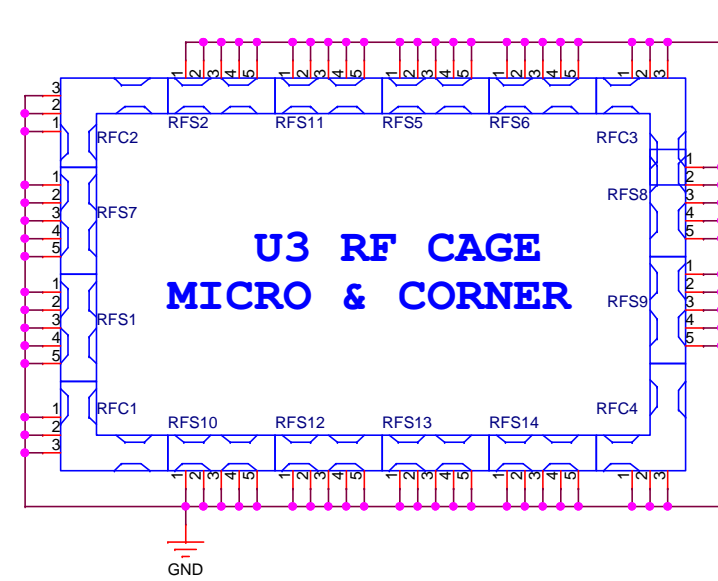
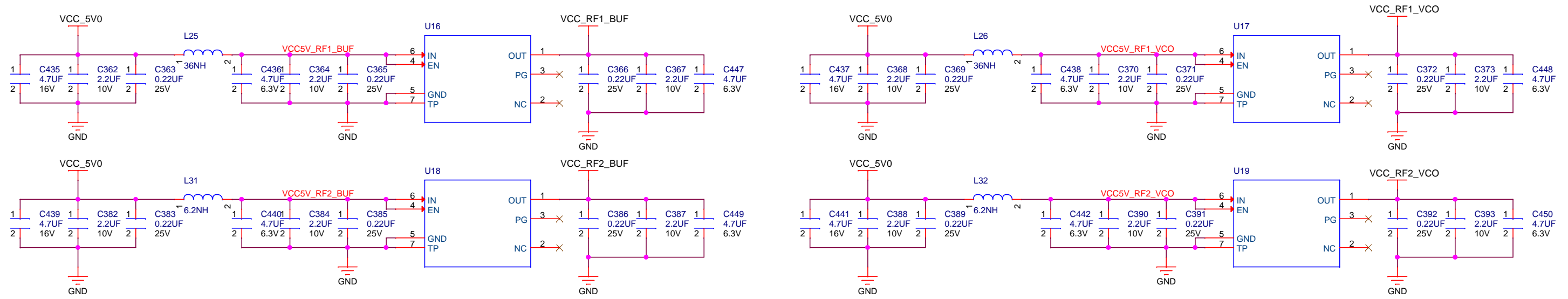





LDO SUPPLY

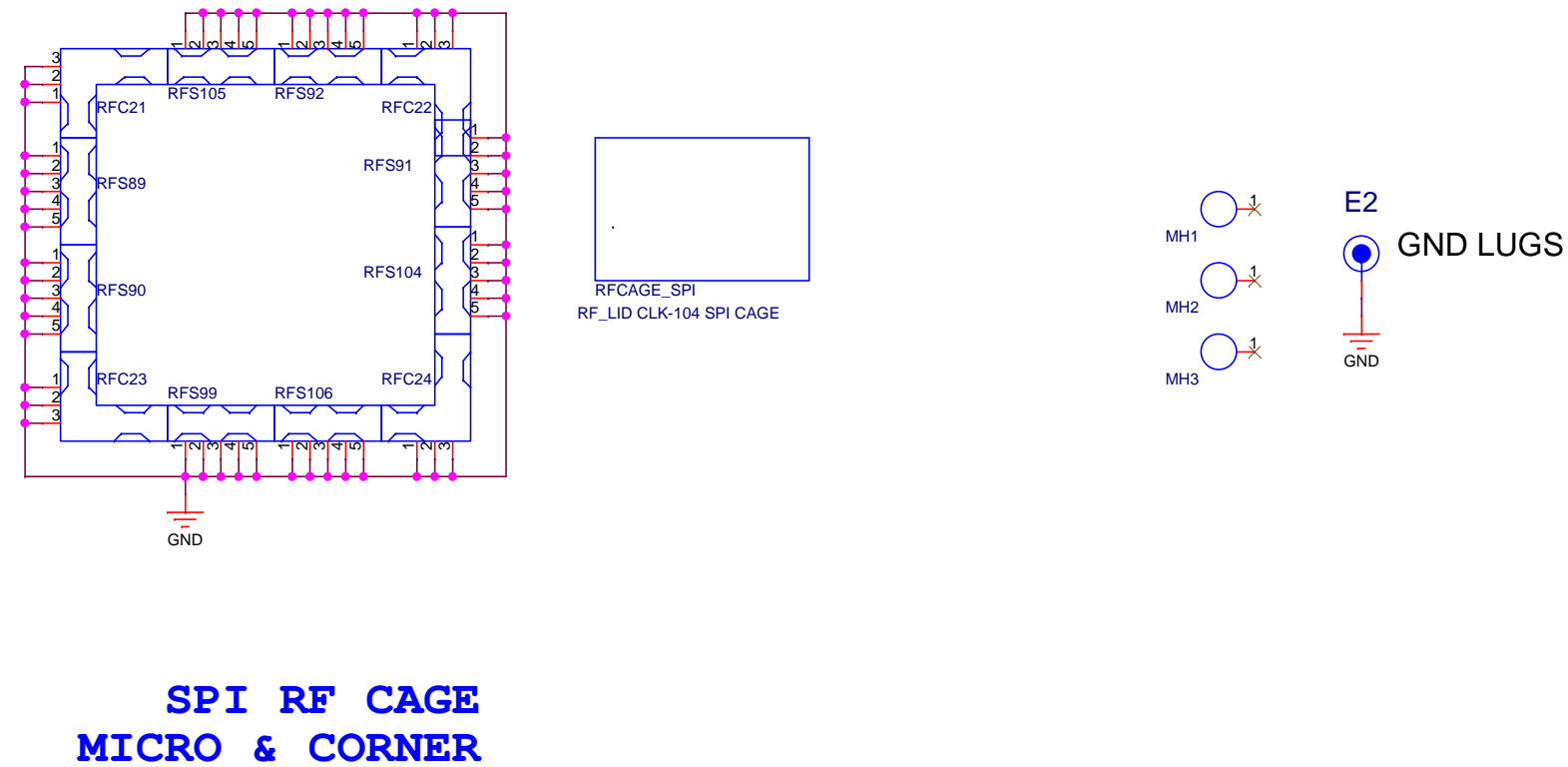
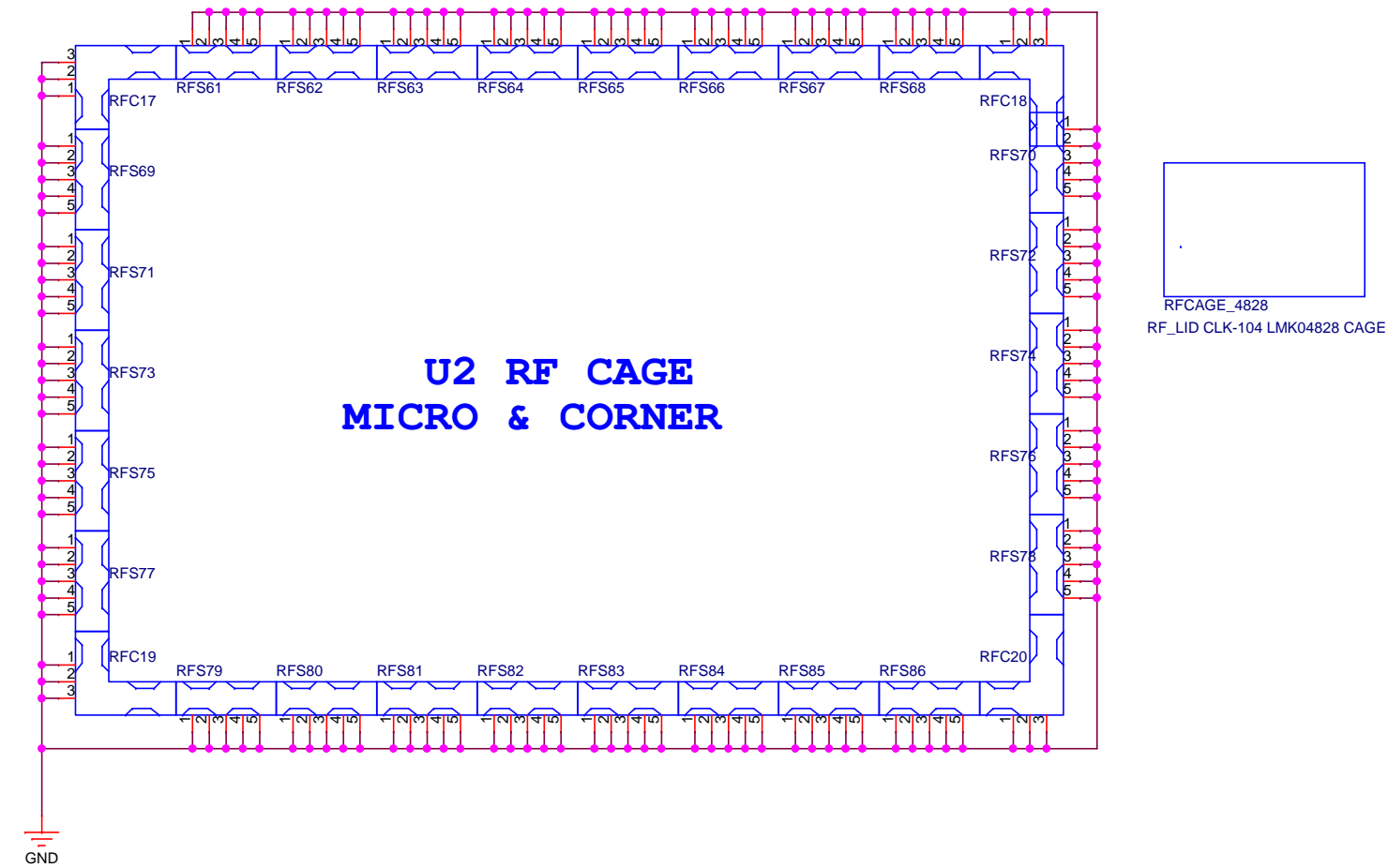



LDO & MECHANICAL



 2100 LOGIC DRIVE SAN JOSE CA			VECTRON	
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MECHANICAL



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